ETSVL004- 2017- Optimal VLSI Delay Tuning by Space Tapering With Clock-Tree Application

Abstract

Interconnect shielding is used in very large scale integration designs to prevent noise interference from the cross-coupling capacitance between adjacent signals. This paper takes advantage of the shields already present in the design and uses them to tune the propagation delay of the clock signals by space tapering, thus eliminating expensive and process variation sensitive dedicated delay buffers. The problem of obtaining the desired delay at a minimum shielding cost (silicon area) by tapering its spacing from the signal wires is solved. A clock-tree synthesis methodology that uses shields to obtain useful skews at the underlying flip-flops is proposed. The method was tested on an industrial 28-nm memory controller and ARM® processor designs, operated in 800-MHz and 1.6-GHz clock speed, respectively, and confirmed its viability for delivering the required useful skews to flip-flops. About 90% of the useful skew problems could be solved by shielding manipulations.